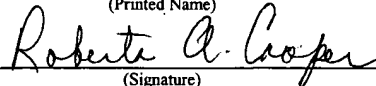


Atty. Dkt. No. 039153-0460 (G1165)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Buynoski et al.  
Title: METHOD OF SELF-  
ANNEALING CONDUCTIVE  
LINES THAT SEPARATES  
GRAIN SIZE EFFECTS FROM  
ALLOY MOBILITY  
Appl. No.: 10/628,733  
Filing Date: 07/28/2003  
Examiner: Joannie A. Garcia  
Art Unit: 2823  
Conf. No.: 4021

<b>CERTIFICATE OF EXPRESS MAILING</b>	
I hereby certify that this correspondence is being deposited with the United States Postal Service's "Express Mail Post Office To Addressee" service under 37 C.F.R. § 1.10 on the date indicated below and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
EV 505573021 US	08/25/04
(Express Mail Label Number)	(Date of Deposit)
Roberta A. Cooper	
(Printed Name)	
	
(Signature)	

**DECLARATION UNDER 37 C.F.R. § 1.131**

Commissioner for Patents  
PO Box 1450  
Alexandria, Virginia 22313-1450

Sir:

We, Matthew S. Buynoski, Connie Pin-Chin Wang, Paul R. Besser, and Minh Q. Tran state and declare that:

1. Each of us is an inventor of at least one of Claims 1-20 currently pending in U.S. Patent Application No. 10/628,733 titled "METHOD OF SELF-ANNEALING CONDUCTIVE LINES THAT SEPARATES GRAIN SIZE EFFECTS FROM ALLOY MOBILITY" (hereinafter "the '733 application").

2. We understand that in an Office Action dated July 8, 2004, each of Claims 1-20 were rejected as being unpatentable in view of U.S. Patent No. 6,660,633 to Lopatin et al. titled "METHOD OF REDUCING ELECTROMIGRATION IN A COPPER LINE BY ELECTROPLATING AN INTERIM COPPER-ZINC ALLOY THIN FILM ON A COPPER SURFACE AND A SEMICONDUCTOR DEVICE THEREBY FORMED" (hereinafter "Lopatin et al.").

3. We understand based on the information provided on the front page of Lopatin et al. that Lopatin et al. has a filing date of February 26, 2002.

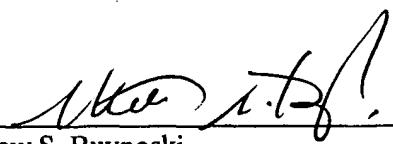
4. At least by August 21, 2001, we conceived in the United States the ideas set forth in Claims 1-20 of the '733 application. Such conception is evidenced by the attached

Exhibit A, which is an invention disclosure form pertaining to the subject matter of the present application.

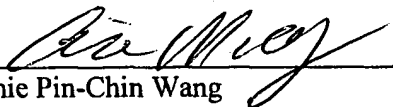
5. Based on the conception of the ideas set forth in Claims 1-20 at least by August 21, 2001, the subject matter recited in Claims 1-20 was invented by us prior to the February 26, 2002 filing date of Lopatin et al.

6. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application or any patent issuing therefrom.

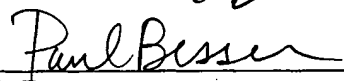
Date: 12 August 2004

By:   
Matthew S. Buynoski


Date: 8/23/04

By:   
Connie Pin-Chin Wang

Date: 8/18/04

By:   
Paul R. Besser

Date: 8/23/04

By:   
Minh Q. Tran

TUESDAY, AUGUST 21, 2001  
 COPPER ALLOY PATENT HARVESTING SESSION  
 GROUP 1: ROOM C-667  
 Technical Leader: Connie Wang  
 TOPIC: PROCESS

PRIORITY  
 A ☐ B ☒  
 C ☐ D ☐

## AMD INVENTION DISCLOSURE

TLD ID#

61165

Rec'd date

Sunnyvale x42110, return to MS68,

Texas x55964 return to MS562

Project: ☐, Product: ☐, Process: ☐, Technology ☐, to which the invention applies (identify):

List 2 to 5 key words useful to search by to find patents or art related to this invention:

Working title of invention: *Separating Cu grain size effects from alloy mobility by use of self-annealing!*

→INVENTOR/SESSION PARTICIPANT ADDRESS INFORMATION IS ON THE NEXT PAGE (IA)←

Inventor's signature: \_\_\_\_\_ date: \_\_\_\_\_  
 Inventor's printed full name: *Matthew Buynoski* Citizenship: \_\_\_\_\_  
 Employee #: \_\_\_\_\_ Extension: \_\_\_\_\_ Mail stop: \_\_\_\_\_ Home telephone: ( ) \_\_\_\_\_  
 Division: \_\_\_\_\_ Directorate: \_\_\_\_\_ Dept #: \_\_\_\_\_ Dept: \_\_\_\_\_ Manager: \_\_\_\_\_  
 Residence address: \_\_\_\_\_  
 Post Office address: \_\_\_\_\_

Co-Inventor's signature: \_\_\_\_\_ date: \_\_\_\_\_  
 Co-Inventor's printed full name: \_\_\_\_\_ Citizenship: \_\_\_\_\_  
 Employee #: \_\_\_\_\_ Extension: \_\_\_\_\_ Mail stop: \_\_\_\_\_ Home telephone: ( ) \_\_\_\_\_  
 Division: \_\_\_\_\_ Directorate: \_\_\_\_\_ Dept #: \_\_\_\_\_ Dept: \_\_\_\_\_ Manager: \_\_\_\_\_  
 Residence address: \_\_\_\_\_  
 Post Office address: \_\_\_\_\_

Co-Inventor's signature: \_\_\_\_\_ date: \_\_\_\_\_  
 Co-Inventor's printed full name: \_\_\_\_\_ Citizenship: \_\_\_\_\_  
 Employee #: \_\_\_\_\_ Extension: \_\_\_\_\_ Mail stop: \_\_\_\_\_ Home telephone: ( ) \_\_\_\_\_  
 Division: \_\_\_\_\_ Directorate: \_\_\_\_\_ Dept #: \_\_\_\_\_ Dept: \_\_\_\_\_ Manager: \_\_\_\_\_  
 Residence address: \_\_\_\_\_  
 Post Office address: \_\_\_\_\_

Co-Inventor's signature: \_\_\_\_\_ date: \_\_\_\_\_  
 Co-Inventor's printed full name: \_\_\_\_\_ Citizenship: \_\_\_\_\_  
 Employee #: \_\_\_\_\_ Extension: \_\_\_\_\_ Mail stop: \_\_\_\_\_ Home telephone: ( ) \_\_\_\_\_  
 Division: \_\_\_\_\_ Directorate: \_\_\_\_\_ Dept #: \_\_\_\_\_ Dept: \_\_\_\_\_ Manager: \_\_\_\_\_  
 Residence address: \_\_\_\_\_  
 Post Office address: \_\_\_\_\_

List on additional sheet if there are more co-inventors and list total number of inventors here: \_\_\_\_\_  
 Name(s) of attorney(s) preferred by inventor(s) to prepare patent application, if known:

LAW FIRM: FOLEY & LARDNER  
 ATTORNEYS: Paul Hunter and Joe Ziebert

Witness 1 initial: \_\_\_\_\_ Witness 2 initial: \_\_\_\_\_

TDG-Copper Alloy Patent Harvesting Session  
Group 1 Topic: Process Issues

Technical Leader: Pin-Chin Connie Wang  
Law Firm: Foley & Lardner (Paul Hunter & Joe Ziebert)

# PARTICIPANT ADDRESSES

Tuesday, August 21, 2001—ROOMS C-6&7

Name	Citizenship	Employee #	Dept. #	Mail Stop	Work #	Fax #	Address	City	State	Zip Code
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Wang, Pin-Chin Connie Connie.Wang@amd.com	TAIWAN	025191	07198	117	408/749-2687	408/749-5144	461 Burgess Drive #2	Menlo Park	CA	94025
You, Lu Lu.You@amd.com	PEOPLE'S REPUBLIC OF CHINA	023537	07198	160	408/749-6589	408/749-5144	5978 Friar Way	San Jose	CA	95129

IDF PAGE 1A

**AMD INVENTION DISCLOSURE**

TLD ID# \_\_\_\_\_

Rec'd date \_\_\_\_\_

California x42110, return to MS68,

Texas x55964 return to MS562,

Dresden x83401 Silke Kretzschmar at MS E21-PP.

Identify known relevant art (patents, publications, products):

Cu is well known to self-anneal at room temp  
Following electroplated deposition

State the problem solved by this invention:

Blocking of ~~the~~ electronic motion by alloying elements in Cu crossing grain boundaries ~~is~~ dependent on both Cu grain size + alloying element diffusion kinetics. This separates them.

Brief description and/or sketch of invention (please attach copies of AMD patent notebook pages, reports or drawings):

Instead of using a furnace at typ 250-350°C to anneal Cu guidetips, the Cu metal is "self-annealed" at ambient from ambient temperature for 24-48 hrs to <100°C for 8-24 hrs. There is no appreciable motion of alloying element when the ~~process~~ Cu re-crystallization occurs. Anneal conditions in subsequent furnace anneal can now be tailored exclusively to needs of distributing the alloying element, without ~~the~~ affecting to Cu grain structure. Also, fewer grain boundaries (post self-anneal) result in a given amt of alloying element being more concentrated in the grain boundaries, requiring use of less alloy element in total to reach an effective level. This leads to lower overall line resistance.

Patent notebook # \_\_\_\_\_

Page numbers \_\_\_\_\_

Number of drawings \_\_\_\_\_

Witness 1 initial: \_\_\_\_\_

Witness 2 initial: \_\_\_\_\_

**AMD INVENTION DISCLOSURE**

TLD ID# \_\_\_\_\_

Rec'd date \_\_\_\_\_

California x42110, return to MS68,

Texas x55964 return to MS562,

Dresden x83401 Silke Kretzschmar at MS E21-PP.

Advantages (check all that apply):

<input type="checkbox"/> avoids existing patent(s)	<input type="checkbox"/> improves precision	<input type="checkbox"/> simplifies manufacturing
<input type="checkbox"/> new function	<input type="checkbox"/> improves accuracy	<input type="checkbox"/> improves wear characteristic
<input type="checkbox"/> improves density	<input type="checkbox"/> improves efficiency	<input type="checkbox"/> improves signal to noise ratio
<input type="checkbox"/> increases operating speed	<input type="checkbox"/> fewer component parts	<input type="checkbox"/>
<input type="checkbox"/> improves reliability	<input type="checkbox"/> reduces cost of manufacturing	<input type="checkbox"/>

Discussion of advantage of the invention over other solutions

(emphasize technical advance in the art as measured against known art): \_\_\_\_\_

First written description* of invention, date: _____	First external disclosure to (name): _____
Date of first drawing*: _____	Date of first external disclosure, none <input type="checkbox"/>
Date invention first reduced to practice: _____	External disclosure under NDA* No <input type="checkbox"/> Yes <input type="checkbox"/>
Made by (name): _____	First external disclosure or use by: presentation <input type="checkbox"/>
Tested by (name): _____	announcement <input type="checkbox"/> sample <input type="checkbox"/> sale <input type="checkbox"/> other <input type="checkbox"/>
Date of first computer simulation: _____	Date of Non-Disclosure Agreement*, if any: _____
Date of first successful test: _____	Date of first publication*: _____
any of above occurred outside of USA <input type="checkbox"/>	Publication name: _____
* attach copy if possible	Date of first commercial use: _____

Does plan exist to publish, disclose or sell? If so, where and when? \_\_\_\_\_

Was invention conceived, constructed or tested pursuant to the performance under a development contract with another company: No ☐ Yes ☐. If yes, company name \_\_\_\_\_

If yes, name of AMD business contact and contract no. \_\_\_\_\_

Was invention jointly developed with participation of inventors from outside AMD: No ☐ Yes ☐.

If yes, Company name \_\_\_\_\_

I have read and understood this disclosure and read and signed each page of the attachments:

Witness 1 signature: \_\_\_\_\_ Date: \_\_\_\_\_  
 Printed name: \_\_\_\_\_ Employee #: \_\_\_\_\_

Witness 2 signature: \_\_\_\_\_ Date: \_\_\_\_\_  
 Printed name: \_\_\_\_\_ Employee #: \_\_\_\_\_

~~After completing to this point, deliver to department reviewer, date delivered: \_\_\_\_\_~~

Witness 1 initial: \_\_\_\_\_ Witness 2 initial: \_\_\_\_\_

**AMD INVENTION DISCLOSURE**

TLD ID# \_\_\_\_\_

Rec'd date \_\_\_\_\_

California x42110, return to MS68,

Texas x55964 return to MS62,

Dresden x83401 Silke Kretzschmar at MS E21-PP.

**DISCLOSURE EVALUATION** (Entries from this point on are by the Reviewer)

Does this invention add value to the AMD intellectual property portfolio? Yes ☐, No ☐.

Explain: \_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

Do you know of any relevant art? Yes ☐, No ☐, If yes, attach a copy and explain: \_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

What application(s) do you foresee for this invention? \_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

I estimate the Value\* of this invention disclosure is A ☐, B ☐, C ☐, D ☐.

\* use worksheet "Valuing Invention Disclosures and Patents".

it is ☐, is not ☐ recommended to AMD for U.S. patent application filing,

it is ☐, is not ☐ recommended to AMD for foreign patent application filing,

it is ☐, is not ☐ recommended to be held as an AMD trade secret,

Give this high priority ☐, normal ☐, low priority ☐, in patent application writing.

**GUIDELINES AND CONSIDERATIONS FOR FOREIGN FILING DECISION**

Filing foreign patent applications is costly. We should choose to do it only when conditions warrant.

**ALL CONDITIONS BELOW MUST APPLY IN ORDER TO INITIATE A FOREIGN FILING:**

- *Invention is High-Valued (A, B)\*, and*
- *Invention is in our technology path (usage), and*
- *Invention usage is detectable by inspection of product, and*
- *Invention is relatively hard to design around, and*
- *Competitor is operating in the country of interest. ( see ca000000.xls tabulation of "Factory Sites outside the USA .)*

I recommend filing patent applications in foreign countries checked below:

Japan <input type="checkbox"/>	S.Korea <input type="checkbox"/>	Taiwan <input type="checkbox"/>	U.K. <input type="checkbox"/>	France <input type="checkbox"/>	Germany <input type="checkbox"/>
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Reviewer's signature: \_\_\_\_\_ Employee #: \_\_\_\_\_ Date: \_\_\_\_\_

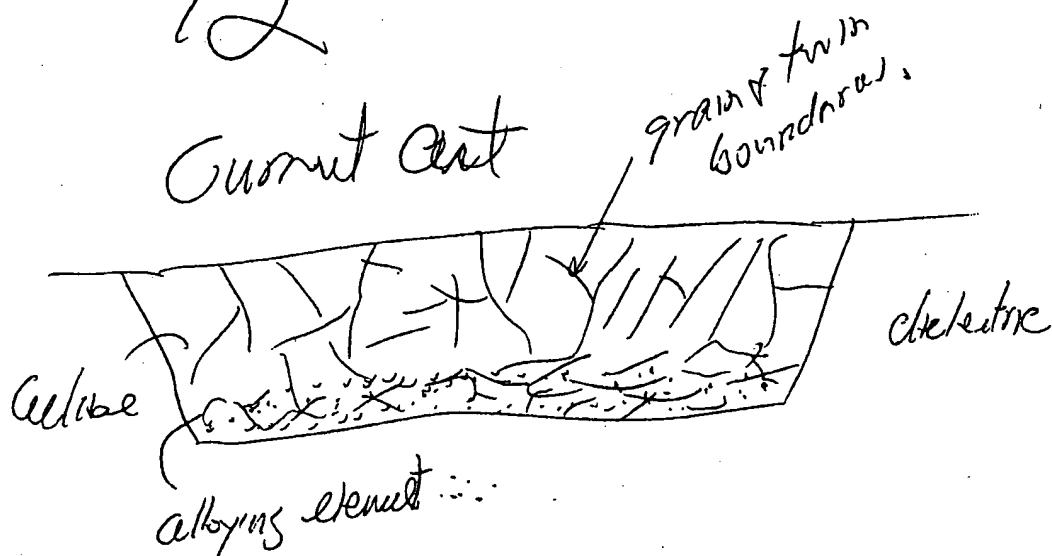
Reviewer's printed name: \_\_\_\_\_

If foreign filing is checked, route to Div. VP for signature.

VP or Designate approves foreign filing (signature) \_\_\_\_\_

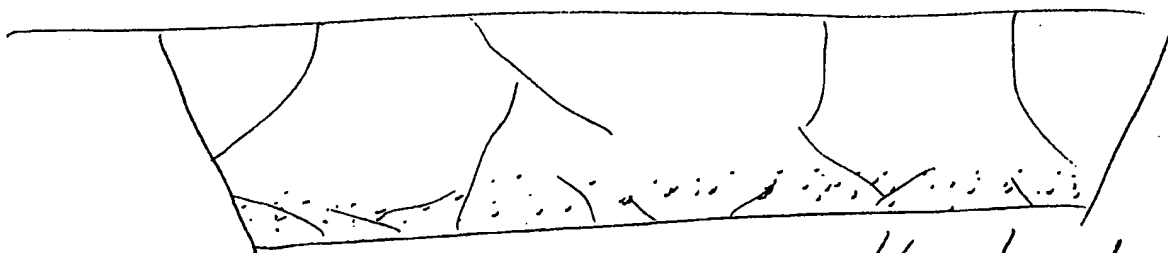
Reviewer: Complete this page and send disclosures to TLD for patent application filing.

#72



Alloying element moves up large # of grain bdrns  
 & may prevent some from being destroyed during anneal.

Proposed — see line after self-anneal



Alloying element has fewer grain/twin boundaries to  
 fill up & passivate. Overall, fewer boundaries mean less  
 chance for grain/body diffusion.